

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

## Refine Search

### Search Results -

Terms	Documents
L31 and prefetch\$	0

**Database:**

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

**Search:**

L32

**Refine Search**

**Recall Text** 

**Clear**

**Interrupt**

### Search History

**DATE:** Wednesday, May 12, 2004    [Printable Copy](#)    [Create Case](#)

#### Set Name Query

side by side

#### Hit Count Set Name

result set

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L32</u>	L31 and prefetch\$	0	<u>L32</u>
<u>L31</u>	5361337.pn.	1	<u>L31</u>
<u>L30</u>	L28 and (cache\$ near9 miss\$)	17	<u>L30</u>
<u>L29</u>	L28 and (reduc\$ or eliminat\$ or minimi\$) near4 (cache\$ near9 miss\$)	0	<u>L29</u>
<u>L28</u>	L27 and switch\$	189	<u>L28</u>
<u>L27</u>	(context\$ near5 resum\$)	234	<u>L27</u>
<u>L26</u>	11 and (context\$ same resum\$)	1	<u>L26</u>
<u>L25</u>	12 and (context\$ same resum\$)	1	<u>L25</u>
<u>L24</u>	13 and (context\$ same resum\$)	0	<u>L24</u>
<u>L23</u>	14 and (context\$ same resum\$)	0	<u>L23</u>
<u>L22</u>	116 and (context\$ same resum\$)	0	<u>L22</u>
<u>L21</u>	16 and (context\$ same resum\$)	760	<u>L21</u>
<u>L20</u>	L19 and context	1	<u>L20</u>
<u>L19</u>	L18	1	<u>L19</u>

<u>L18</u>	6237073.pn.	1	<u>L18</u>
<u>L17</u>	6,047,363.pn.	1	<u>L17</u>
<u>L16</u>	L15 and (thread\$ or process\$)	5	<u>L16</u>
<u>L15</u>	14 and (context\$ near5 switch\$)	5	<u>L15</u>
<u>L14</u>	17 and (context\$ near5 switch\$)	0	<u>L14</u>
<u>L13</u>	17 and (memory\$ near4 referenc\$) and critical\$	1	<u>L13</u>
<u>L12</u>	17 and (critical\$ and memory\$) and referenc\$	1	<u>L12</u>
<u>L11</u>	17 and (critical\$ same memory\$) same referenc\$	0	<u>L11</u>
<u>L10</u>	17 and (critical\$ near4 memory\$) same referenc\$	0	<u>L10</u>
<u>L9</u>	L7 and (prefetch\$ same compil\$)	1	<u>L9</u>
<u>L8</u>	L7 and prefetch\$	1	<u>L8</u>
<u>L7</u>	5784711.pn.	1	<u>L7</u>
<u>L6</u>	5,471,602.pn.	1	<u>L6</u>
<u>L5</u>	L4 and (critical\$ near8 memory\$)	2	<u>L5</u>
<u>L4</u>	L2 and (prefetch\$ near8 memory\$) near5 (compil\$ or execut\$)	39	<u>L4</u>
<u>L3</u>	L2 and (prefetch\$ near8 memory\$)	111	<u>L3</u>
<u>L2</u>	(reduc\$ or eliminat\$) near4 cache\$ near9 miss\$	565	<u>L2</u>
<u>L1</u>	THOMPSON, CAROL.IN.	13	<u>L1</u>

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
L1 and (sequen\$ or index\$)	1

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L29

Refine Search

Recall Text 

Clear

Interrupt

### Search History

DATE: Wednesday, May 12, 2004    [Printable Copy](#)    [Create Case](#)

#### Set Name Query

side by side

#### Hit Count Set Name

result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L29</u>	11 and (sequen\$ or index\$)	1	<u>L29</u>
<u>L28</u>	l26 and (constant\$ same start\$ same register\$)	1	<u>L28</u>
<u>L27</u>	L26 and count\$	0	<u>L27</u>
<u>L26</u>	3571804.pn.	1	<u>L26</u>
<u>L25</u>	L22 and prefetch\$	1	<u>L25</u>
<u>L24</u>	L22 and prefetch\$ and count\$	0	<u>L24</u>
<u>L23</u>	L22 and sequential\$ and prefetch\$ and count\$	0	<u>L23</u>
<u>L22</u>	(constant near4 start\$ near9 register\$)	89	<u>L22</u>
<u>L21</u>	l11 and (constant\$ or start\$) near5 register\$	0	<u>L21</u>
<u>L20</u>	11 and (constant\$ or start\$) near5 register\$	0	<u>L20</u>
<u>L19</u>	11 and prefetch\$ near9 (count\$ or number\$ or times\$)	1	<u>L19</u>
<u>L18</u>	11 and (execut\$ or process\$) near9 prefetch\$	1	<u>L18</u>
<u>L17</u>	L1 and operating system	0	<u>L17</u>
<u>L16</u>	11 and (location\$ or address\$)	1	<u>L16</u>

<u>L15</u>	l1 and (prefetch\$ near9 (code\$ or program\$ Or software\$ or modul\$))	1	<u>L15</u>
<u>L14</u>	(critical\$ near4 memory\$ near4 referenc\$)	24	<u>L14</u>
<u>L13</u>	l11 and critical\$	0	<u>L13</u>
<u>L12</u>	L11 and context and switch and resum\$	1	<u>L12</u>
<u>L11</u>	5361337.pn.	1	<u>L11</u>
<u>L10</u>	l1 and (stor\$ or sav\$ or memory\$) near9 prefetch\$	1	<u>L10</u>
<u>L9</u>	l1 and prefetch\$ near9 (memory\$ near9 referenc\$)	1	<u>L9</u>
<u>L8</u>	l1 and (exchang\$ or switch\$)	1	<u>L8</u>
<u>L7</u>	l6 and critical\$	1	<u>L7</u>
<u>L6</u>	l1 and (process\$ or thread\$ or execut\$)	1	<u>L6</u>
<u>L5</u>	L4 and prefetch\$	1	<u>L5</u>
<u>L4</u>	l1 and (memory\$ near9 referenc\$) and critical\$	1	<u>L4</u>
<u>L3</u>	L1 and prefetch\$ and memory and compil\$ and (execut\$ or process\$)	1	<u>L3</u>
<u>L2</u>	L1 and prefetch\$ and memory and compil\$	1	<u>L2</u>
<u>L1</u>	5784711.pn.	1	<u>L1</u>

END OF SEARCH HISTORY

## Refine Search

### Search Results -

Terms	Documents
(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	1

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L41

Refine Search

Recall Text

Clear

Interrupt

### Search History

 DATE: Wednesday, May 12, 2004    [Printable Copy](#)    [Create Case](#)

<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
<i>DB=TDBD; PLUR=YES; OP=ADJ</i>			
<u>L41</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	1	<u>L41</u>
<i>DB=DWPI; PLUR=YES; OP=ADJ</i>			
<u>L40</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	1	<u>L40</u>
<i>DB=JPAB; PLUR=YES; OP=ADJ</i>			
<u>L39</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	<u>L39</u>
<i>DB=EPAB; PLUR=YES; OP=ADJ</i>			
<u>L38</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	<u>L38</u>
<i>DB=USOC; PLUR=YES; OP=ADJ</i>			

<u>L37</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	<u>L37</u>
<i>DB=PGPB; PLUR=YES; OP=ADJ</i>			
<u>L36</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	21	<u>L36</u>
<u>L35</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	<u>L35</u>
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L34</u>	710/262.ccls.	211	<u>L34</u>
<u>L33</u>	711/2,3,113,169.ccls.	1714	<u>L33</u>
<u>L32</u>	717/151,140,141,127,128.ccls.	849	<u>L32</u>
<u>L31</u>	L30 and (constant\$ and start\$ and register\$)	1	<u>L31</u>
<u>L30</u>	3571804.pn.	1	<u>L30</u>
<u>L29</u>	l1 and (sequen\$ or index\$)	1	<u>L29</u>
<u>L28</u>	l26 and (constant\$ same start\$ same register\$)	1	<u>L28</u>
<u>L27</u>	L26 and count\$	0	<u>L27</u>
<u>L26</u>	3571804.pn.	1	<u>L26</u>
<u>L25</u>	L22 and prefetch\$	1	<u>L25</u>
<u>L24</u>	L22 and prefetch\$ and count\$	0	<u>L24</u>
<u>L23</u>	L22 and sequential\$ and prefetch\$ and count\$	0	<u>L23</u>
<u>L22</u>	(constant near4 start\$ near9 register\$)	89	<u>L22</u>
<u>L21</u>	l11 and (constant\$ or start\$) near5 register\$	0	<u>L21</u>
<u>L20</u>	l1 and (constant\$ or start\$) near5 register\$	0	<u>L20</u>
<u>L19</u>	l1 and prefetch\$ near9 (count\$ or number\$ or times\$)	1	<u>L19</u>
<u>L18</u>	l1 and (execut\$ or process\$) near9 prefetch\$	1	<u>L18</u>
<u>L17</u>	L1 and operating system	0	<u>L17</u>
<u>L16</u>	l1 and (location\$ or address\$)	1	<u>L16</u>
<u>L15</u>	l1 and (prefetch\$ near9 (code\$ or program\$ Or software\$ or modul\$))	1	<u>L15</u>
<u>L14</u>	(critical\$ near4 memory\$ near4 referenc\$)	24	<u>L14</u>
<u>L13</u>	l11 and critical\$	0	<u>L13</u>
<u>L12</u>	L11 and context and switch and resum\$	1	<u>L12</u>
<u>L11</u>	5361337.pn.	1	<u>L11</u>
<u>L10</u>	l1 and (stor\$ or sav\$ or memory\$) near9 prefetch\$	1	<u>L10</u>
<u>L9</u>	l1 and prefetch\$ near9 (memory\$ near9 referenc\$)	1	<u>L9</u>
<u>L8</u>	l1 and (exchang\$ or switch\$)	1	<u>L8</u>
<u>L7</u>	l6 and critical\$	1	<u>L7</u>
<u>L6</u>	l1 and (process\$ or thread\$ or execut\$)	1	<u>L6</u>
<u>L5</u>	L4 and prefetch\$	1	<u>L5</u>
<u>L4</u>	l1 and (memory\$ near9 referenc\$) and critical\$	1	<u>L4</u>
<u>L3</u>	L1 and prefetch\$ and memory and compil\$ and (execut\$ or process\$)	1	<u>L3</u>
<u>L2</u>	L1 and prefetch\$ and memory and compil\$	1	<u>L2</u>
<u>L1</u>	5784711.pn.	1	<u>L1</u>



[Subscribe \(Full Service\)](#) [Register \(Limited Service, Free\)](#) [Login](#)

Search: ☒ The ACM Digital Library ☐ The Guide

prefetch and memory reference and reduce and miss and cache



THE ACM DIGITAL LIBRARY



[Feedback](#) [Report a problem](#) [Satisfaction survey](#)

Terms used

**prefetch** and **memory reference** and **reduce** and **miss** and **cache** and **context** and **switch**

Found **57,023** of **132,857**

Sort results by

relevance



[Save results to a Binder](#)

[Try an Advanced Search](#)

[Try this search in The ACM Guide](#)

Display results

expanded form



[Search Tips](#)

☐ Open results in a new window

Results 1 - 20 of 200

Result page: [1](#) [2](#) [3](#) [4](#) [5](#) [6](#) [7](#) [8](#) [9](#) [10](#) [next](#)

Best 200 shown

Relevance scale ☐ ☐ ☐ ☐ ☐

1 [Comparative evaluation of latency reducing and tolerating techniques](#)

Anoop Gupta, John Hennessy, Kourosh Gharachorloo, Todd Mowry, Wolf-Dietrich Weber  
April 1991 **ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture**, Volume 19 Issue 3

Full text available: pdf(1.36 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

2 [Reducing memory latency via non-blocking and prefetching caches](#)

Tien-Fu Chen, Jean-Loup Baer  
September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems**, Volume 27 Issue 9

Full text available: pdf(1.36 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Hardware-software trade-offs in a direct Rambus implementation of the RAMpage memory hierarchy](#)

Philip Machanick, Pierre Salverda, Lance Pompe  
October 1998 **Proceedings of the eighth international conference on Architectural support for programming languages and operating systems**, Volume 32 , 33 Issue 5 , 11

Full text available: pdf(1.47 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The RAMpage memory hierarchy is an alternative to the traditional division between cache and main memory: main memory is moved up a level and DRAM is used as a paging device. The idea behind RAMpage is to reduce hardware complexity, if at the cost of software complexity, with a view to allowing more flexible memory system design. This paper investigates some issues in choosing between RAMpage and a conventional cache architecture, with a view to illustrating trade-offs which can be made in choosi ...

4 [Instruction prefetching of systems codes with layout optimized for reduced cache misses](#)

Chun Xia, Josep Torrellas  
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd**



## Refine Search

### Search Results -

Terms	Documents
(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	1

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L41

Refine Search

Recall Text

Clear

Interrupt

### Search History

 DATE: Wednesday, May 12, 2004    [Printable Copy](#)    [Create Case](#)

Set Name	Query	Hit Count	Set Name
side by side			result set
	DB=TDDB; PLUR=YES; OP=ADJ		
L41	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	1	L41
	DB=DWPI; PLUR=YES; OP=ADJ		
L40	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	1	L40
	DB=JPAB; PLUR=YES; OP=ADJ		
L39	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	L39
	DB=EPAB; PLUR=YES; OP=ADJ		
L38	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	L38
	DB=USOC; PLUR=YES; OP=ADJ		

<u>L37</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	<u>L37</u>
<i>DB=PGPB; PLUR=YES; OP=ADJ</i>			
<u>L36</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	21	<u>L36</u>
<u>L35</u>	(reduc\$ or eliminat\$ or minimi\$) near5 (cache\$ near9 miss\$) and prefetch\$ and (memory\$ near9 referenc\$)	0	<u>L35</u>
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L34</u>	710/262.ccls.	211	<u>L34</u>
<u>L33</u>	711/2,3,113,169.ccls.	1714	<u>L33</u>
<u>L32</u>	717/151,140,141,127,128.ccls.	849	<u>L32</u>
<u>L31</u>	L30 and (constant\$ and start\$ and register\$)	1	<u>L31</u>
<u>L30</u>	3571804.pn.	1	<u>L30</u>
<u>L29</u>	l1 and (sequen\$ or index\$)	1	<u>L29</u>
<u>L28</u>	l26 and (constant\$ same start\$ same register\$)	1	<u>L28</u>
<u>L27</u>	L26 and count\$	0	<u>L27</u>
<u>L26</u>	3571804.pn.	1	<u>L26</u>
<u>L25</u>	L22 and prefetch\$	1	<u>L25</u>
<u>L24</u>	L22 and prefetch\$ and count\$	0	<u>L24</u>
<u>L23</u>	L22 and sequential\$ and prefetch\$ and count\$	0	<u>L23</u>
<u>L22</u>	(constant near4 start\$ near9 register\$)	89	<u>L22</u>
<u>L21</u>	l11 and (constant\$ or start\$) near5 register\$	0	<u>L21</u>
<u>L20</u>	l1 and (constant\$ or start\$) near5 register\$	0	<u>L20</u>
<u>L19</u>	l1 and prefetch\$ near9 (count\$ or number\$ or times\$)	1	<u>L19</u>
<u>L18</u>	l1 and (execut\$ or process\$) near9 prefetch\$	1	<u>L18</u>
<u>L17</u>	L1 and operating system	0	<u>L17</u>
<u>L16</u>	l1 and (location\$ or address\$)	1	<u>L16</u>
<u>L15</u>	l1 and (prefetch\$ near9 (code\$ or program\$ Or software\$ or modul\$))	1	<u>L15</u>
<u>L14</u>	(critical\$ near4 memory\$ near4 referenc\$)	24	<u>L14</u>
<u>L13</u>	l11 and critical\$	0	<u>L13</u>
<u>L12</u>	L11 and context and switch and resum\$	1	<u>L12</u>
<u>L11</u>	5361337.pn.	1	<u>L11</u>
<u>L10</u>	l1 and (stor\$ or sav\$ or memory\$) near9 prefetch\$	1	<u>L10</u>
<u>L9</u>	l1 and prefetch\$ near9 (memory\$ near9 referenc\$)	1	<u>L9</u>
<u>L8</u>	l1 and (exchang\$ or switch\$)	1	<u>L8</u>
<u>L7</u>	l6 and critical\$	1	<u>L7</u>
<u>L6</u>	l1 and (process\$ or thread\$ or execut\$)	1	<u>L6</u>
<u>L5</u>	L4 and prefetch\$	1	<u>L5</u>
<u>L4</u>	l1 and (memory\$ near9 referenc\$) and critical\$	1	<u>L4</u>
<u>L3</u>	L1 and prefetch\$ and memory and compil\$ and (execut\$ or process\$)	1	<u>L3</u>
<u>L2</u>	L1 and prefetch\$ and memory and compil\$	1	<u>L2</u>
<u>L1</u>	5784711.pn.	1	<u>L1</u>